What is claimed is:

1. A path detection apparatus comprising:

a peak detection section that detects a peak value of a delay profile created by a received signal sampled with a predetermined sampling number chip by chip;

a comparison section that compares power values between adjacent samples of said delay profile; and

a path selection section that selects, when the power value compared by said comparison section increases or decreases consecutively up to the kth (k is a natural number of 2 or greater) forward or backward from the sample having said peak value, said kth sample as a path.

2. The path detection apparatus according to claim 1, further comprising a path limitation section that selects a path selected by said path selection section whose power value is equal to or greater than a threshold as a path to be used for demodulation.

3. The path detection apparatus according to claim 1, wherein said path selection section selects a sample of the same sampling number as said sample number delayed for a 1-chip time from the sample of said peak value as a path.

4. A reception apparatus provided with a path detection apparatus, said path detection apparatus comprising:

a peak detection section that detects a peak value of a delay profile created by a received signal sampled with a predetermined sampling number chip by chip;

a comparison section that compares power values between adjacent samples of said delay profile; and

a path selection section that selects, when the power value compared by said comparison section increases or decreases consecutively up to the kth (k is a natural number of 2 or greater) forward or backward from the sample having said peak value, said kth sample as a path.

5. A demodulation apparatus provided with a path detection apparatus, said path detection apparatus comprising:

a peak detection section that detects a peak value of a delay profile created by a received signal sampled with a predetermined sampling number chip by chip;

a comparison section that compares power values between adjacent samples of said delay profile; and

a path selection section that selects, when the power value compared by said comparison section increases or decreases consecutively up to the kth (k is a natural number of 2 or greater) sample forward or backward from the sample having said peak value, said kth sample as a path.

6. A path detection method comprising:

a step of detecting a peak value of a delay profile created by a received signal sampled with a predetermined

sampling number chip by chip;

a comparison step of comparing power values of adjacent samples of said delay profile; and

a path selection step of selecting, when the compared power value increases or decreases consecutively up to the kth (k is a natural number of 2 or greater) sample forward or backward from the sample having said peak value, said kth sample as a path.